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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/313,037	05/17/1999	LOUIS M. MELI	PHN-17.438	3381

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	16

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/313,037	MELI, LOUIS M.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dallas Semiconductor "DS87C550 Data Sheet" in view of Palowski US Patent 5,426,769.

In regards to claim 1, Dallas Semiconductor discloses a register circuit for storing at least two addresses in parallel in Figure 1 elements DPTR0 and DPTR1,

an address selector (data pointer select bit SEL page 13 4th paragraph) arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively on page 14 first paragraph,

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states on page 14 first paragraph and table of assembly code.

Dallas Semiconductor however does not disclose a control register that is instruction-settable to respective control states that control whether or not the

processing device updates the at least two addresses will be updated as a side-effect of executing the memory access instruction. Palowski discloses the use of a control special function register (SFR) to enable or disable the auto-increment/auto-increment function of the address SFR in column 14 lines 57 – 61. This SFR is settable by writing to the corresponding address as indicated in column 14 line 59. The control SFR controls multiple addresses as shown in figure 8. Incrementing and decrementing the address SFR is a side-effect to using a move instruction as illustrated in the second table in column 15 (in comparison to first table). Palowski is in the related art of addressing memory in the 8051 series microcontroller, therefore the incorporation of Palowski's auto-increment/auto-increment SFR in Dallas Semiconductor's 87C550 would have been obvious at the time of invention to one of ordinary skill in the art.

In regards to claim 2, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Palowski further discloses each control state specifies respective update actions for all of the at least two addresses in column 14 lines 58 and 59.

In regards to claim 3, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Palowski further discloses the control states specifying a choice of at least no-update, update by incrementing with a predetermined value and update by decrementing with the predetermined value in column 14 lines 61 – 65.

In regards to claim 4, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Palowski further discloses that execution of the memory access instruction further causes the instruction execution unit to perform, upon the

currently selected address, the update action that is specified by the control state of the control register for that one of the at least two addresses that is the currently selected address in column 15 lines 26 – 28.

In regards to claim 5, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Palowski further discloses the instruction set includes a load from memory instruction and store to memory instruction, for causing the execution unit to respond ro the execution the memory access instruction in column 15 lines 22 – 25.

In regards to claim 6, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Applicant discloses as prior art a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively on page 2 lines 6 and 7. Applicant does not disclose the setting the control register to one of the control states that causes both the first one and second one of the address to be updated. Palowski discloses the enable and disable for the auto-increment/auto-decrement may be set individually in column 14 lines 63-65. Therefore it would have been obvious at the time of invention to one of ordinary skill in the art to set both auto-updates for the purpose of moving blocks of data from one memory region to another memory region.

In regards to claim 7, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Applicant discloses as prior art a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses

respectively on page 2 lines 6 and 7. Applicant does not disclose the setting the control register to one of the control states that causes only one of the first one and second one of the address to be updated. Palowski discloses the enable and disable for the auto-increment/auto-decrement may be set individually in column 14 lines 63-65. Therefore it would have been obvious at the time of invention to one of ordinary skill in the art to set only one of the auto-updates for the purpose of transferring blocks of data to and from a memory mapped IO port.

In regards to claim 8, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Dallas Semiconductor further discloses the address selector cycles back and forth between states that select a first and second one of at least two addresses respectively on page 14, first paragraph.

In regards to claim 9, Dallas Semiconductor and Palowski disclose the invention substantially as claimed. Palowski further discloses each of four pages having an address and data SFR, given Dallas Semiconductor's motivation of improved efficiency of data moves given on page 13, first paragraph of "Dual Data Pointer With Inc/Dec"; it would have been obvious at the time of invention to one of ordinary skill in the art to include additional address registers one for each extra address SFR in order to improve the efficiency of inter-page data transfers. By incorporation of Palowski within Dallas Semiconductor the user would be able to cycle through selected states of the address SFR with the ability of incrementing or decrementing each address.

In regards to claim 10, Dallas Semiconductor discloses a register circuit for storing at least two addresses in parallel in Figure 1 elements DPTR0 and DPTR1,

an address selector including a register selector register (data pointer select bit SEL page 13 4th paragraph) and a logic circuit (inherent to perform cycling operation) collectively arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively on page 14 first paragraph,

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states on page 14 first paragraph and table of assembly code.

Dallas Semiconductor however does not disclose a control register in communication with said register selector register and said control register being instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses will be updated as a side-effect of executing the memory access instruction. Palowski discloses the use of a control special function register (SFR) to enable or disable the auto-increment/auto-increment function of the address SFR in column 14 lines 57 – 61. This SFR is settable by writing to the corresponding address as indicated in column 14 line 59. The control SFR controls multiple addresses as shown in figure 8. Incrementing and decrementing the address SFR is a side-effect to using a move instruction as illustrated in the second table in column 15 (in comparison to first table). Palowski is in the related art of

addressing memory in the 8051 series microcontroller, therefore the incorporation of Palowski's auto-increment/auto-increment SFR in Dallas Semiconductor's 87C550 would have been obvious at the time of invention to one of ordinary skill in the art.

Response to Arguments

Applicant's arguments filed 12 February 2003 have been fully considered but they are not persuasive. Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of invention to combine Palowski, US Patent 5,426,769, with Dallas Semiconductor "DS87C550 EPROM High-Speed Micro with ADC and PWM" as shown in the prior office action (and above). Since the combination of these two prior arts is obvious, the double incorporation of Palowski in Dallas Semiconductor is also obvious. In other words, if it is obvious to make one of the data pointer registers disclosed in Dallas Semiconductor, auto-increment/auto-decrement as disclosed by Palowski, it would likewise be obvious to have the second data pointer register auto-increment/auto-decrement as well.

Therefore the examiner respectfully maintains the 35 U.S.C §103(a) rejection on claims 1 - 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone

number for the organization where this application or proceeding is assigned is (703)746-7238.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

PB

Mano Padmanabhan
1/12/04
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 2100